



Token Bit Manager:

The Next Step in Particle Detection

A. Armstrong & W. Behn (Mentor: Dr. A. Ivanov)

Department of Physics, Kansas State University, Manhattan, Kansas 66506-2501, USA

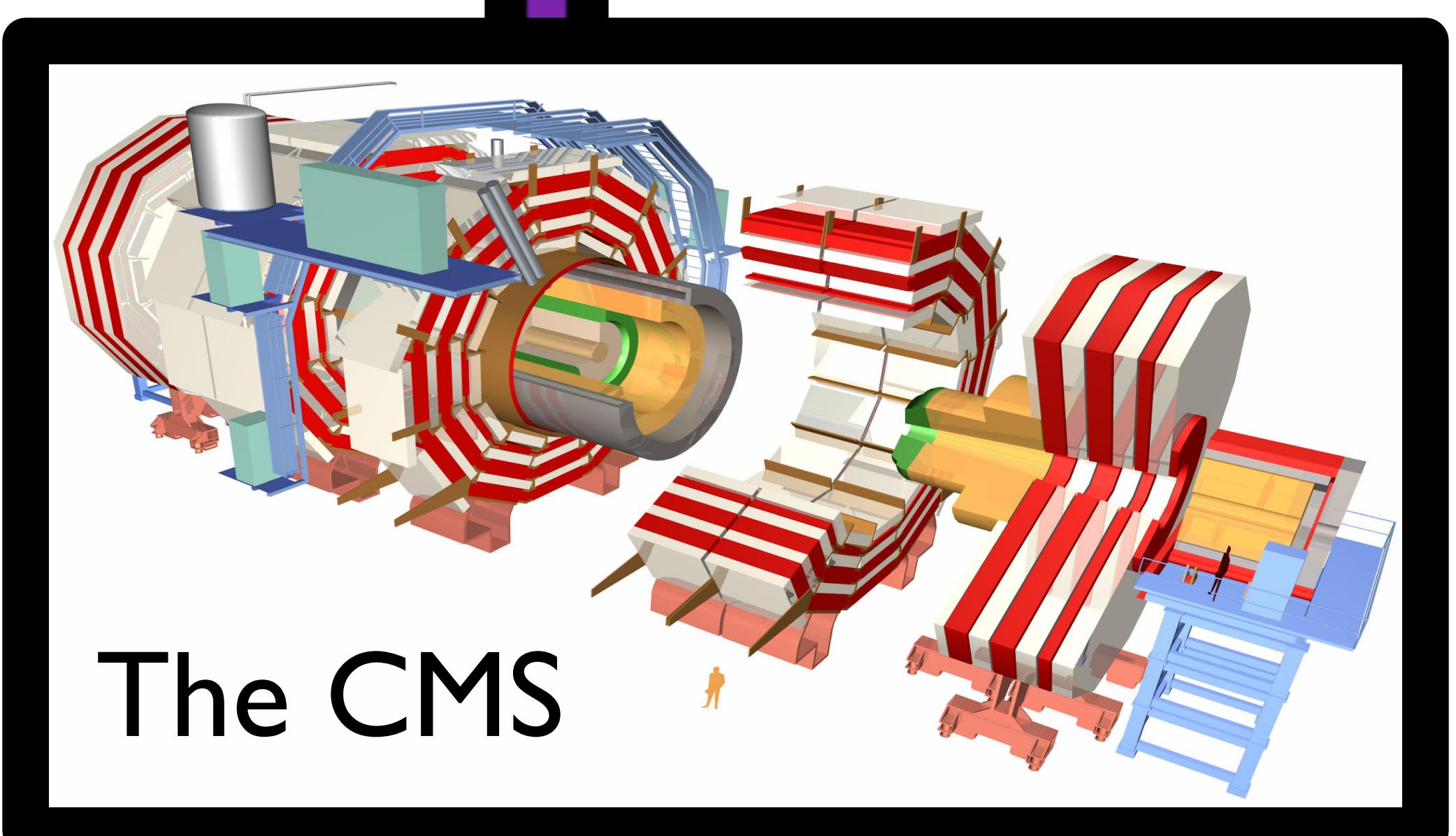


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Introduction

In 2017, the CMS will undergo upgrades to dramatically improve the detectors ability to probe the foundations of the physical world. Many of these upgrades deal with projected increases in beam luminosity which ultimately produces more data to be sifted, recorded, and analyzed. Key to managing all the data will be the TBM 08b and 09 chips stationed inches away from the collision point that handle communication between the data taken in the innermost layers of the detector and all other electronics. With massive increases in the amount of data output at the LHC, the new TBM's improved speed, control, endurance, and functionality will be essential.

During the summer of 2014, KSU was tasked with testing the new TBM chips to guarantee they can get the job done. All chips that were tested passed at least minimum requirements. Information on each chip's performance was sent off with the chips to other labs for radiation testing.



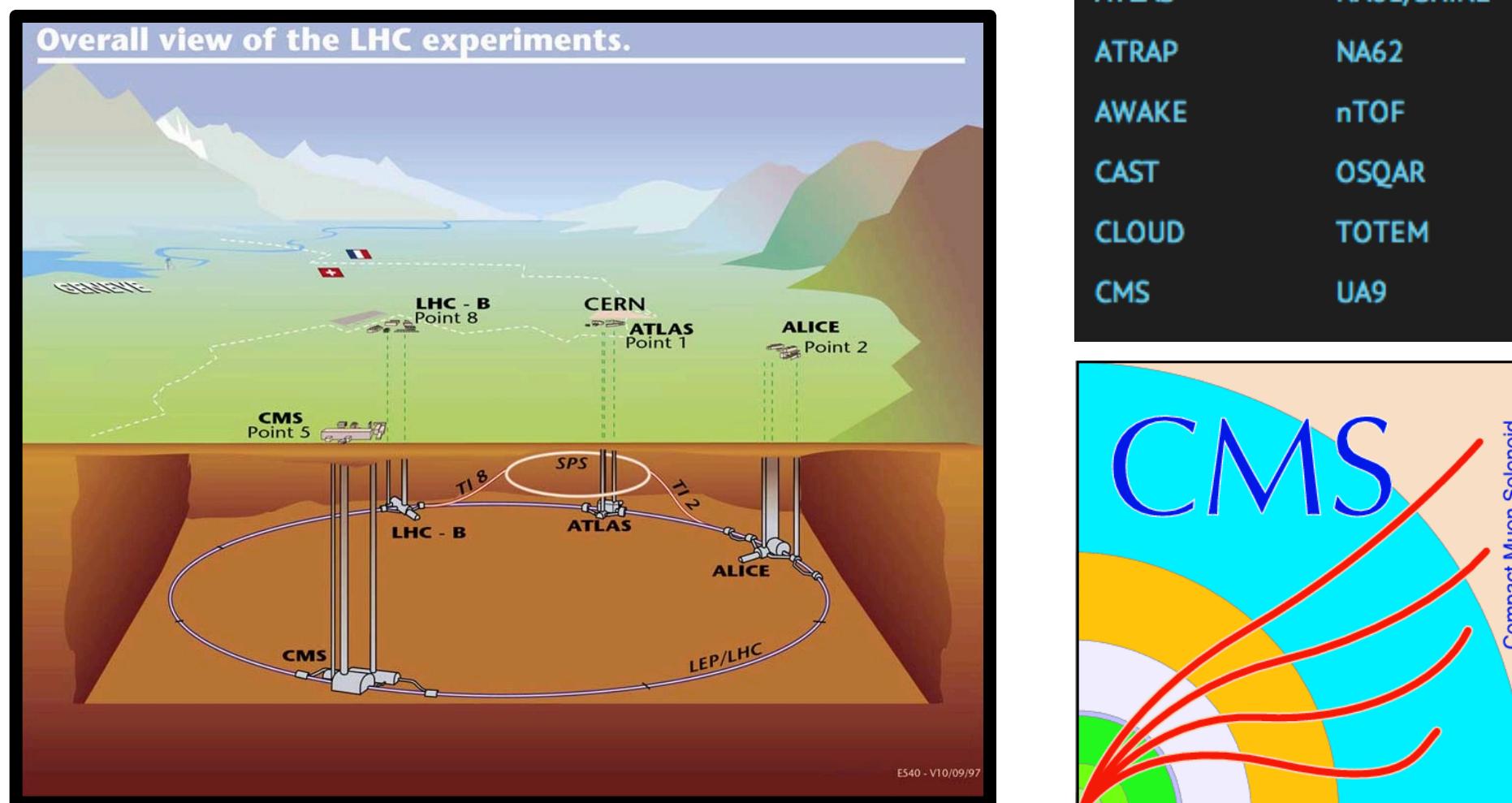
The CMS

CMS Overview

European Council of Nuclear Research (CERN) – council overseeing dozens of experiments in fundamental physics at several accelerators and other facilities (see right)

Large Hadron Collider (LHC) – the largest particle accelerator in the world, which collides protons at high energies to study the debris at one of four detectors (see below)

Compact Muon Solenoid (CMS) – an extremely compact set of detectors layered around an LHC collision point that uses a solenoid magnet, muon detectors, and several other systems to track movement and energy of the particles released during collisions (see left)



CERN Labs	
ACCELERATORS	
The Antiproton Decelerator	
The Large Hadron Collider	
The Proton Synchrotron	
The Super Proton Synchrotron	
CERN Neutrinos to Gran Sasso	
EXPERIMENTS	
ACE	COMPASS
AEGIS	DIRAC
ALICE	ISOLDE
ALPHA	LHCb
AMS	LHCf
ASACUSA	MOEDAL
ATLAS	NA61/SHINE
ATRAP	NA62
AWAKE	nTOF
CAST	OSQAR
CLOUD	TOTEM
CMS	UA9

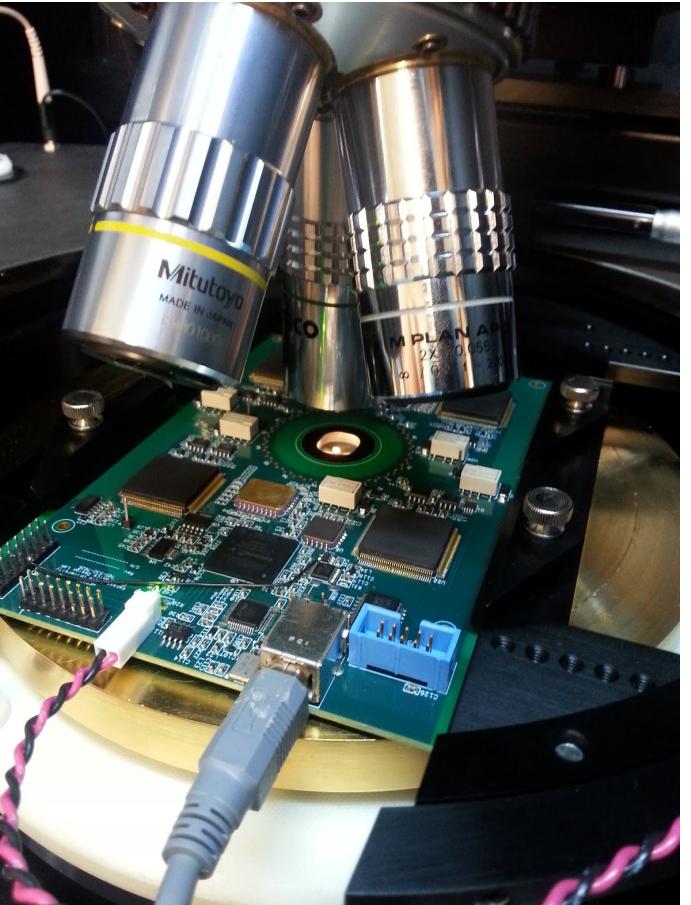
Testing

The Setup:

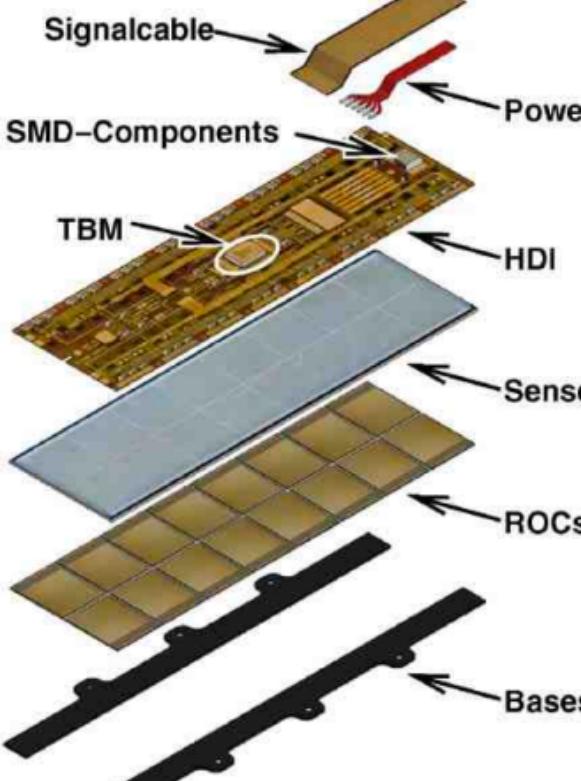
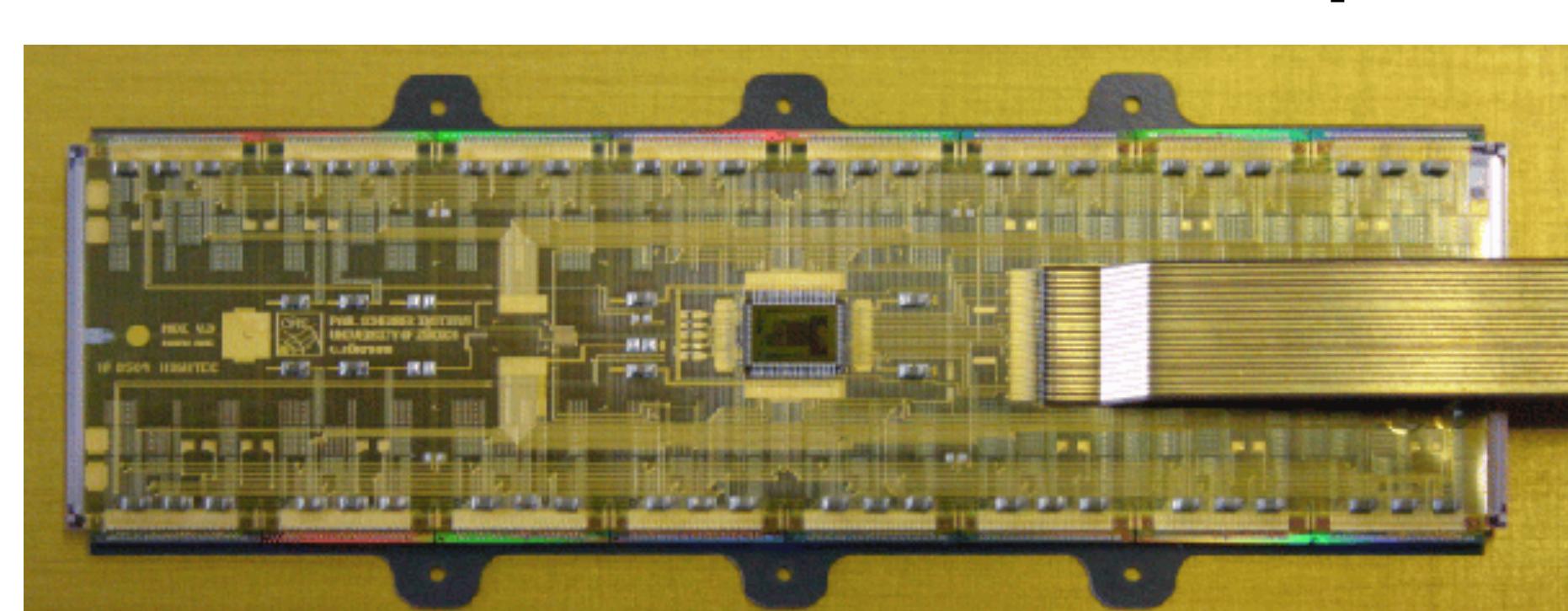
- ❑ Clean testing environment – reduces potential damage or contamination to TBMs
- ❑ Cascade hardware with Nucleus 3.2 software – Nucleus software controls the Cascade probe station
- ❑ Vibraplane table – minimizes vibrations while running tests

Testing Procedure:

- 1) TBM is placed on a platinum alloy stage (see right) that moves beneath a testing board to align and then connect TBM pads with micro probes attached to testing board
- 2) Contact is confirmed by small scratches on the pads visible under a digital microscope (see left)
- 3) Voltage is applied across the testing board
- 4) Testing is carried out by previously written testing code
- 5) Chips are required to pass while operating at or above 50 MHz overclocking. This ensures that the TBMs can operate at the required 40 MHz for a long time as radiation damage slowly lowers peak operating speed



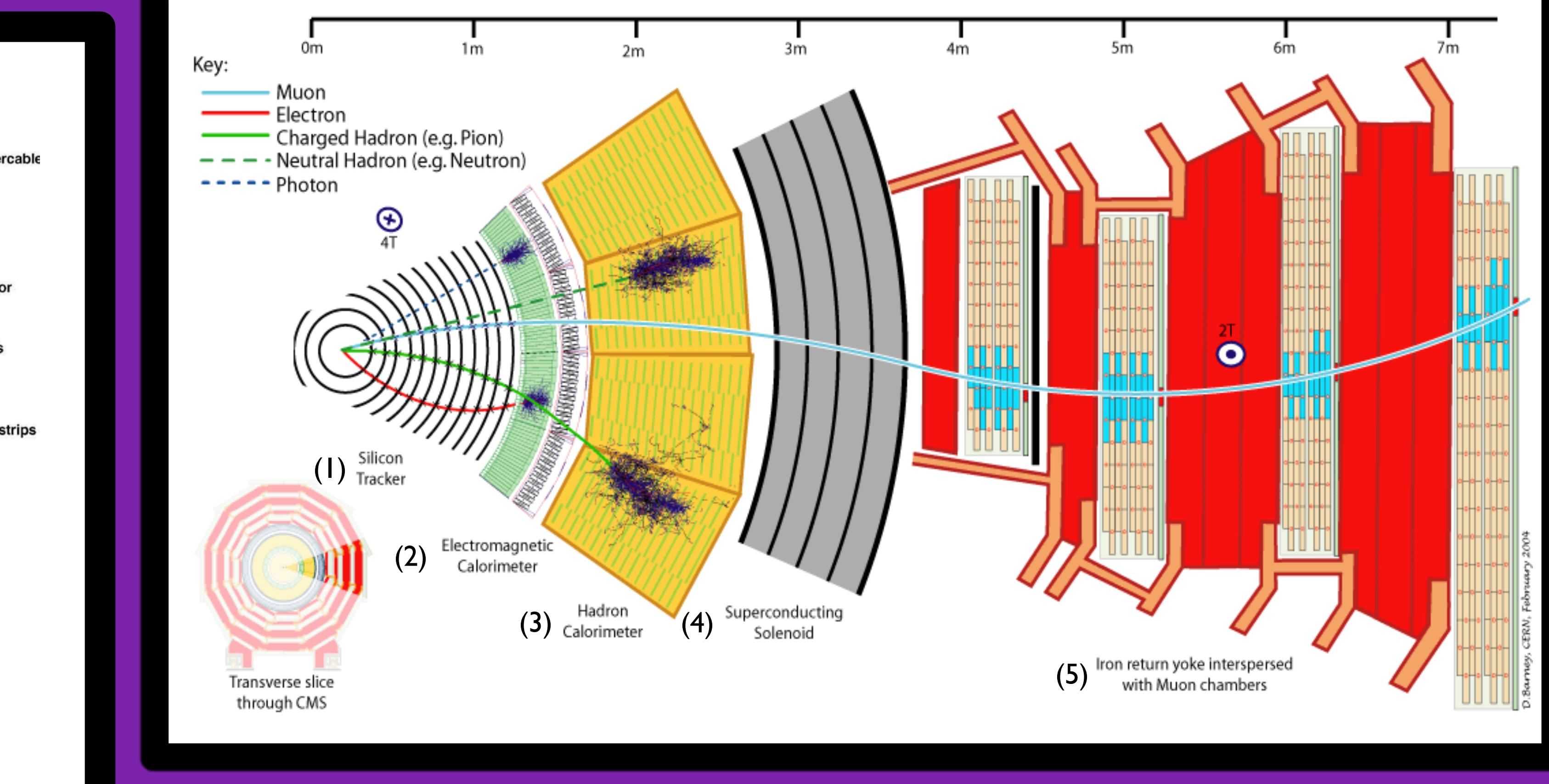
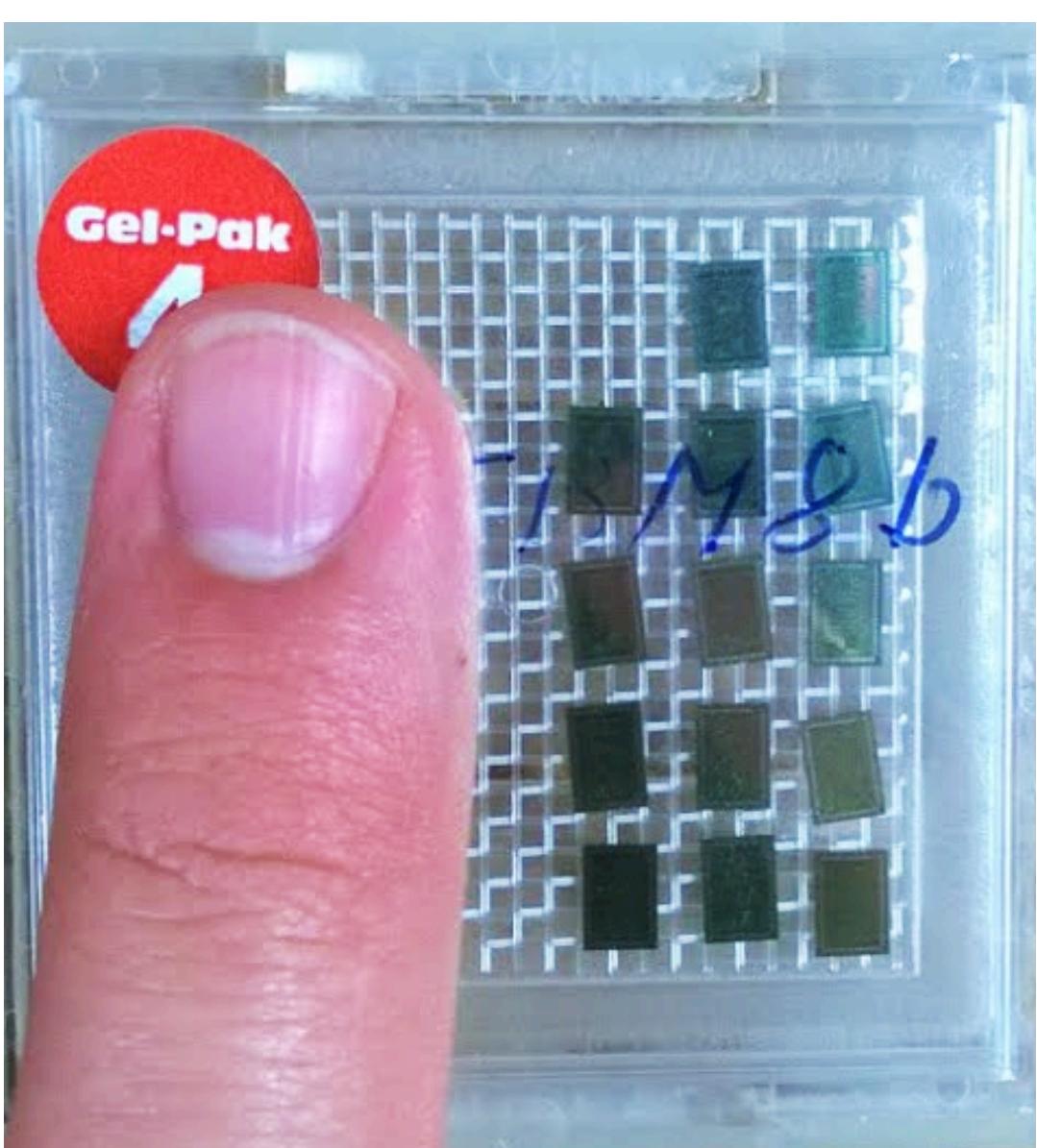
TBM Chip



- ❑ Modules (see above): Major subunits of inner silicon tracker containing pixel sensors, 8-16 Read-Out Chips (ROCs), a TBM, and all other supporting hardware.

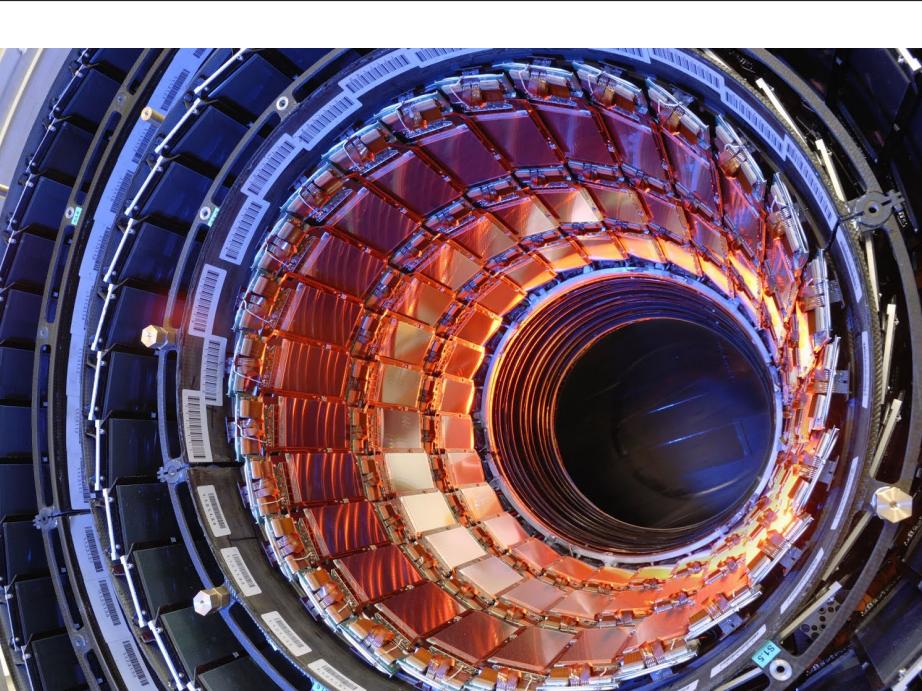
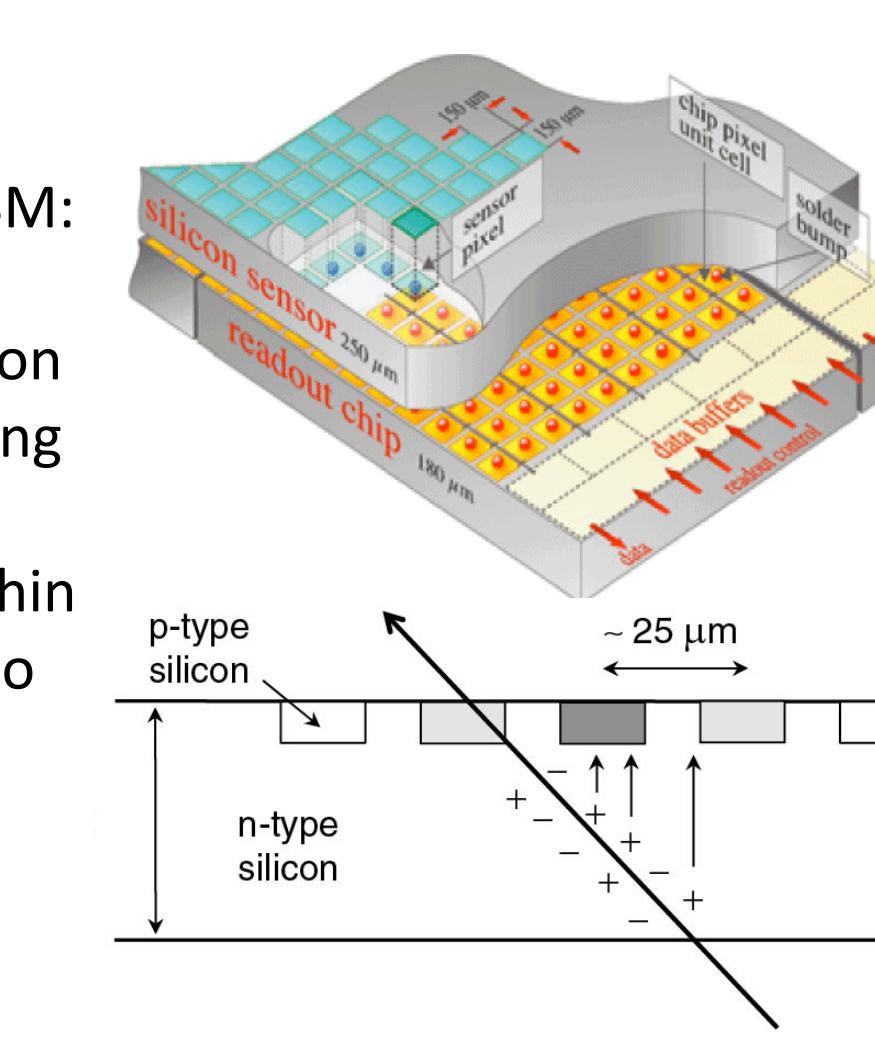
TBM Functioning:

- 32-deep stack of buffer allows the trigger system adequate space to store and process accepted data before being sent downstream for more detailed analysis
- Normally the buffer stack is empty in order to accommodate the burst rates from noise or high track density events
- TBMs are in charge of synchronizing the clocks of the ROCs which is crucial for reconstructing particle paths and syncing data acquisition



ROCs and Pixels

- 1) Particles released in collision pass through a series of semiconductor pixel detectors (see lower left) located in the innermost detector layers (see right)
 - 2) Pixel data transferred to and stored in ROC (see left)
 - 3) ROCs store event information in the buffer until receiving a trigger signal via the TBM token
- ❑ The TBM-ROC trigger signals are as follows:
- 111 - Reset Readout Chip: Immediately, all events on the stack are marked No Token Pass as well as for the next 8 cycles.
 - 101 - Reset TBM: Same as above, however the TBM event counter is also set to zero and restarts after 8 clock cycles
 - 100 - Pre-Calibrate/Sync/Reset: A calibration trigger is sent to the ROC/The TBM checks for a clock error/The event counter is set to zero

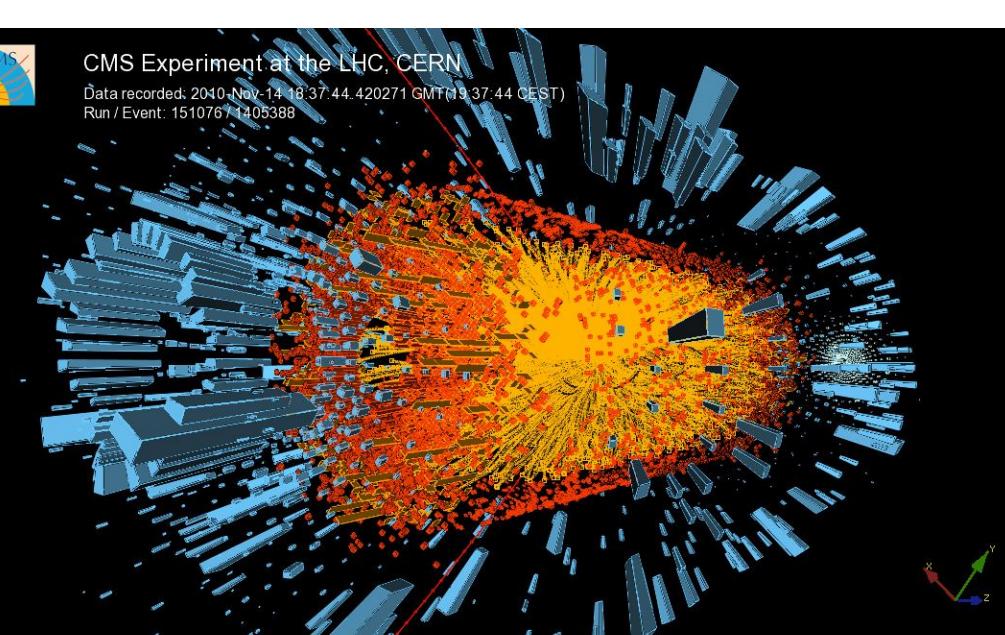


Summary of Benefits

The TBM 09 is a vast improvement over its predecessor. Being digital, the TBM 09 is already a faster chip than the currently used TBM 05a, which is analog.

Additionally, the TBM 09 chip utilizes four TBM cores creating a "quad" core. The ROCs are split between the four TBM cores allowing for a precise ability to reset certain ROCs without resetting all ROCs on the module at once. This allows the TBM 09 a much needed line of communication to the control rooms above the LHC.

Moreover, the TBM 09 is more radiation resistant and made from less material which interferes much less with possible particle detection. Overall, the TBM 09 is a clear upgrade from the current TBM 05a.



Trigger System

The NEED for a Trigger System

- ❑ At 40 million collisions a second, there are 40 Terabytes of data being generated every second. Not all data is valuable
- ❑ The Trigger System sifts through the different pieces of data at every level and selects those that are most likely to reveal something new about physics
- ❑ The Trigger System decreases collision information by a factor of 10 million, still leaving plenty of data for analysis (see right)

The Trigger System Process

- ① Particles pass through ROCs in silicon detectors which record and time-stamp position information
- ② Particles continue through to calorimeters or muon chambers for final measurements
- ③ Automatic processes built into trigger electronics receive data and decide to accept or discard data
- ④ Acceptance/Rejection message is sent down to TBM, which then passes it on to the relevant ROC
- ⑤ If data is accepted, the ROC sends the data back to the TBM, which sends that data out for analysis

